Matching of speed (maximum delay in nanoseconds of passing of signals from inputs on outputs of the circuit) combinatorial circuits II of Altera (D_A) corporation synthesized with help MAX+PLUS and at usage of method M3 of synthesis of two-level combinatorial circuits with various time of creation of output signals ZUBR (D_3) for PLD of CLASSIC set

Name	**L**	**N**	**P**	**D_A**	**D_3**	**D_A/D_3**
9sym	9	1	87	44	44	1,00
Alu4	14	8	1028	270	44	6,14
Apex3	54	50	280	108	44	2,45
Apex4	9	19	438	106	44	2,41
Cps	24	109	654	44	44	1,00
Ex1010	10	10	1024	304	44	6,91
Seq	41	35	1459	122	44	2,77
Table3	14	14	175	54	44	1,23
Z9sym	9	1	420	272	44	6,18
mid						3,34