Matching of speed (maximum delay in nanoseconds of passing of signals from inputs on outputs of the circuit) combinatorial circuits of II Altera (D_A) corporation synthesized with help MAX+PLUS and at usage of method M2 of synthesis of single-level combinatorial circuits with usage of mounting connection of outputs PLD on OR ZUBR (D_2) for PLD of FLEX 10K set

Name	**L**	**N**	**P**	**D_A**	**D_2**	**D_A/D_2**
9sym	9	1	87	33	20,2	1,63
B12	15	9	431	19,9	16,5	1,21
Cps	24	109	654	57	59,3	0,96
Inc	7	9	34	22,8	19	1,20
Pdc	16	40	1280	48,4	25,5	1,90
Z9sym	9	1	420	38,1	20,2	1,89
mid						1,47