Matching of speed (maximum delay in nanoseconds of passing of signals from inputs on outputs of the circuit) combinatorial circuits II of Altera C_A) corporation synthesized with help MAX+PLUS and at usage of method M2 of synthesis of single-level combinatorial circuits with usage of mounting connection of outputs PLD on OR ZUBR (C_2) for PLD of MAX 7000 set

Name	**L**	**N**	**P**	**D_A**	**D_2**	**D_A/D_2**
9sym	9	1	87	15,5	6	2,58
Alu4	14	8	1028	51,5	12,5	4,12
Apex3	54	50	280	37,5	15	2,50
Apex4	9	19	438	79,9	12,5	6,39
Ex1010	10	10	1024	102,3	7,5	13,64
Z9sym	9	1	420	31,6	6	5,27
mid						5,75