Matching of speed (maximum delay in nanoseconds of passing of signals from inputs on outputs of the circuit) combinatorial circuits synthesized with the help of MAX+PLUS II of Altera (D_A) corporation and at usage of method M2 of synthesis of single-level combinatorial circuits with usage of mounting connection of outputs PLD on OR ZUBR (D_2) for PLD of CLASSIC set

Name	**L**	**N**	**P**	**D_A**	**D_2**	**D_A/D_2**
9sym	9	1	87	44	20	2,20
Alu4	14	8	1028	270	20	13,50
Apex3	54	50	280	108	22	4,91
Apex4	9	19	438	106	20	5,30
Cps	24	109	654	44	22	2,00
Ex1010	10	10	1024	304	20	15,20
Inc	7	9	34	32	20	1,60
Seq	41	35	1459	122	22	5,55
Z9sym	9	1	420	272	20	13,60
mid						7,10